LISTING OF CLAIMS

1. (Presently Amended) A non-volatile memory cell comprising:

a substantially single crystalline semiconductive material of a first conductivity type, having a substantially planar surface with a trench in said surface of said material; said trench having a sidewall and a bottom wall;

a first region of a second conductive type, different from said first conductivity type in said material along said planar surface;

a second region of a second conductive type in said material along said bottom wall of said trench;

a channel region, having a first portion and a second portion, connecting said first and second regions for the conduction of charges, wherein said first portion is along said surface adjacent to said first region, and said second portion is along said sidewall adjacent to said second region;

a dielectric on said channel region;

a floating gate in said trench, on said dielectric, spaced apart from said second portion of said channel region;

a first gate electrode on said dielectric, spaced apart from said first portion of said channel region; and

a second gate electrode, in said trench, capacitively coupled to said floating gate, and to said second region.

2. (Original) The cell of claim 1 wherein said substantially single crystalline semiconductive material is single crystalline silicon.

3. (Original) The cell of claim 1 wherein said floating gate having a tip substantially adjacent to said first gate electrode.

4. (Original) The cell of claim 3 further comprising a second dielectric between said tip and said first gate electrode permitting the Fowler-Nordheim tunneling of electrons from said floating gate to said first gate electrode.

5. (Original) The cell of claim 1 further comprising a second dielectric between said floating gate and said bottom wall of said trench permitting the Fowler-Nordheim tunneling of electrons from said floating gate to said second region.

6. (Presently Amended) An array of non-volatile memory cells, arranged in a plurality of rows and columns, said array comprising:

a substantially single crystalline semiconductive material of a first conductivity type, having a substantially planar surface with a plurality of trenches in said surface of said material; each of said trenches having a sidewall and a bottom wall;

a plurality of non-volatile memory cells arranged in a plurality of rows and columns in said semiconductive substrate material with each cell comprising:

a first region of a second conductive type, different from said first conductivity type in said material along said surface;

a second region of said second conductive type in said material along said bottom wall of said trench;

a channel region, having a first portion and a second portion, connecting said first and second regions for the conduction of charges, wherein said first portion is along said surface adjacent to said first region, and said second portion is along said sidewall adjacent to said second region;

a dielectric on said channel region;

a floating gate on said dielectric, spaced apart from said second portion of said channel region;

a first gate electrode on said dielectric, spaced apart from said first portion of said channel region; and

a second gate electrode, in said trench, capacitively coupled to said floating gate, and to said second region;

wherein said cells in the same row have said first gate electrode in common;

wherein said cells in the same column have said first region in common, said second region in common, said second gate electrode in common; and

wherein said cells in adjacent columns have said first region in common to one side; and said second gate electrode and said second region in common to another side.

7. (Original) The array of claim 6 wherein said substantially single crystalline semiconductive material is single crystalline silicon.

8. (Original) The array of claim 6 wherein in each cell the floating gate has a tip substantially adjacent to the first gate electrode.

9. (Original) The array of claim 8 wherein each cell further comprising a second dielectric between said tip and said first gate electrode permitting the Fowler-Nordheim tunneling of electrons from said floating gate to said first gate electrode.

10. (Original) The array of claim 6 wherein each cell further comprising a second dielectric between said floating gate and said bottom wall of said trench permitting the Fowler-Nordheim tunneling of electrons from said floating gate to said second region.

11. (Original) The array of claim 6 wherein an isolation region separates adjacent rows of cells.

12. (Original) A method of manufacturing an array of non-volatile memory cells in a substantially single crystalline semiconductive substrate material of a first conductivity type, wherein said array of non-volatile memory cells has a plurality of non-volatile memory cells

arranged in a a plurality of rows and columns in said semiconductive substrate material, said method comprising:

forming spaced apart isolation regions on said semiconductive substrate that are substantially parallel to one another and extend in said column direction, with an active region between each pair of adjacent isolation regions, wherein said semiconductive substrate has a substantially planar surface;

forming a plurality of memory cells in each of the active regions, wherein the formation of each of the memory cells includes:

forming a trench into the surface of the substrate, said trench having a sidewall and a bottom wall;

forming a floating gate in the trench along the sidewall and insulated therefrom;

forming a first region in said substrate along the bottom wall of the trench, with said first region being of a second conductivity type, different from said first conductivity type;

forming a first gate electrode in the trench, said first gate electrode insulated from said first region and capacitively coupled to said floating gate;

forming a second region, of the second conductivity type in said substrate, along the surface thereof, spaced apart from the trench; and

forming a second gate electrode spaced apart from the surface between said second region and said trench.

13. (Original) The method of claim 12 wherein said step of forming said first gate electrode includes forming said first gate electrode continuously in said row direction across a plurality of columns.

14. (Original) The method of claim 12 wherein said step of forming said second gate electrode includes forming said second gate electrode continuously in said column direction across a plurality of rows.

15. (Original) The method of claim 14 wherein said step of forming said first region and said second region includes forming said first region and said second region continuously in said row direction across a plurality of columns.

16. (Original) The method of claim 15 wherein said cells in the same row have said second gate electrode in common; and wherein said cells in the same column have said first region in common, said second region in common, said first gate electrode in common; and wherein said cell in adjacent columns have said second region in common to one side; and said first gate electrode and said first region in common to another side.

17. (Original) A method of manufacturing a non-volatile memory cell in a substantially single crystalline semiconductive substrate of a first conductivity type, said substrate having a substantially planar surface, said method comprising:

forming a trench into the surface of the substrate, said trench having a sidewall and a bottom wall;

forming a floating gate in the trench along the sidewall and insulated therefrom;

forming a first region in said substrate along the bottom wall of the trench, with said first region being of a second conductivity type, different from said first conductivity type;

forming a first gate electrode in the trench, said first gate electrode insulated from said first region and capacitively coupled to said floating gate;

forming a second region, of the second conductivity type in said substrate, along the surface thereof, spaced apart from the trench; and

forming a second gate electrode spaced apart from the surface between said second region and said trench.

18. (Original) The method of claim 17 further comprising forming an insulation material between the second gate electrode and said floating gate with a thickness that permits Fowler-Nordheim tunneling of electrons from said second floating gate to said second gate electrode.

19. (Original) The method of claim 17 further comprising forming an insulation material between said floating gate and said bottom wall of said trench permitting the Fowler-Nordheim tunneling of electrons from said floating gate to said second region.

20. (Original) The method of claim 18 wherein said step of forming said floating gate includes forming said floating gate above the substrate surface.